Application No.: 10/568,230
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For: Vertical Nano-Transistor...

Current Claims (6 October 2006)

1. (Canceled)

2. (Currently amended) The transistor of claim ~~1~~ 23, in which the semiconductor channel region ~~(3)~~ is structured cylindrically.

3. (Currently amended) The transistor of claim ~~1~~ 23, in which the thickness of the metal film ~~(1)~~ forming the vertical gate region ~~(G)~~ is less than 100 µm, preferably 5 to 20 µm.

4. (Currently amended) The transistor of claim ~~1~~ 23, in which the diameter of the semiconductor channel region ~~(3)~~ is several ten to several hundred nanometers.

5. (Currently amended) The transistor of claim ~~1~~ 23, in which the thickness of the electrical insulation ~~(2)~~ between the gate region ~~(G)~~ and the semiconductor channel ~~(3)~~ is several ten to several hundred nanometers.

6. (Currently amended) The transistor of claim ~~1~~ 23, in which the thickness of the insulation layer ~~(2)~~ on the upper and lower surface of the metal film ~~(1)~~ is several micrometers.

7. (Currently amended) The transistor of claim ~~1~~ 23, wherein the semiconductor channel comprises a material selected from the group consisting of ~~the semiconductor channel (3) is~~ $CuSCN$, ~~or~~ TiO_2, ~~or~~ PbS, ~~or~~ ZnO ~~or~~ and another compound semiconductor.

8. (Currently amended) The transistor of claim ~~1~~ 23,
wherein the ~~material for the~~ source ~~(S)~~ and the drain ~~(D)~~ region comprises a material selected from the group consisting of ~~is~~ Au, ~~or~~ Ag, ~~or~~ Cu, ~~or~~ Ni ~~or~~ and Al.

9. (Currently amended) The transistor of claim ~~1~~ 23,
wherein the source ~~(S)~~ and the drain ~~(D)~~ region are structured as dots.

10. (Currently amended) A memory arrangement, comprising:
a metal film;
~~in which~~ a plurality of vertical nano-transistors according to claim 23 is arranged ~~according to at least one of the preceding claims~~ adjacent each other in ~~a~~ the metal film.

11. (Currently amended) A method of fabricating vertical nano-transistors according to claim 1, including at least the following method steps
- forming holes ~~(4)~~ in a thin metal film ~~(1)~~ constituting the gate region ~~(G)~~ of the transistor, for forming the channel region ~~(3)~~,
- applying insulation material to the walls of the holes ~~(4)~~,
- applying insulation material to the upper and lower surface of the metal film ~~(1)~~,
- applying semiconductor material in the insulated holes ~~(4)~~ for forming the semiconductor channel region ~~(3)~~,
- applying contacts for forming the source ~~(S)~~ and drain ~~(D)~~ regions.

12. (Currently amended) The method of claim 11,
wherein the holes ~~(4)~~ in the metal film ~~(1)~~ are formed by focused ion beams.

13. (Currently amended) The method of claim 11,
wherein the holes ~~(4)~~ in the metal film ~~(1)~~ are formed by a laser beam.

14. (Currently amended) The method of claim 11,

wherein the insulation material is applied to the upper and lower surface of the metal film ~~(1)~~ by thin-film technology.

15. (Currently amended) The method of claim 11,
wherein the insulation material is applied to the wall of the holes ~~(4)~~ and to the upper and lower surface of the metal film ~~(1)~~ by vacuum filtration of a polymer solution.

16. (Currently amended) The method of claim 11,
wherein the insulation material is applied to the wall of the holes ~~(4)~~ and to the upper and lower surface of the metal foil ~~(1)~~ by electro-chemical deposition.

17. (Currently amended) The method of claim 11,
wherein the insulation material is applied to the wall of the holes ~~(4)~~ and to the upper and lower surface of the metal foil ~~(1)~~ by chemical deposition.

18. (Currently amended) The method of claim 11,
wherein the semiconductor channel region comprises a material ~~used for the semiconductor channel region (3) is~~ selected from the group consisting of $CuSCN$, ~~or~~ TiO_2, ~~or~~ PbS, ~~or~~ ZnO ~~or~~ and another compound semiconductor.

19. (Currently amended) The method of claim 11,
wherein the semiconductor material is introduced into the insulated holes ~~(4)~~ by electro-chemical bath precipitation.

20. (Currently amended) The method of claim 11,
wherein the semiconductor material is introduced into the insulated holes ~~(4)~~ by chemical deposition.

21. (Currently amended) The method of claim 11,
wherein the semiconductor material is introduced into the insulated holes ~~(4)~~ by the

ILGAR process.

22. (Currently amended) The method of claim 11,
wherein the source and drain regions comprise a material ~~used for the source and drain region is~~ selected from the group consisting of Au, ~~or~~ Ag, ~~or~~ Cu, ~~or~~ Ni ~~or~~ and Al.

23. (New) A vertical nano-transistor, comprising:

a source region;

a drain region;

a semiconductor channel region intermediate the source region and the drain region;

a gate region comprising a metal film, the transistor being embedded in the metal film such that the gate region and the semiconductor channel region form a coaxial structure and the source region, the semiconductor channel region and the drain region being vertically arranged; and

the gate region being electrically insulated from the source region, the drain region and the semiconductor channel region.